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10ES32

Third Semester B.E. Degree Examination, June/July 2018
Analog Electronics Circuits

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Assuming an ideal diode, sketch v_i , v_d and i_d for half-wave rectifier of Fig.1(a). The input is a sinusoid with frequency 50 Hz. (08 Marks)

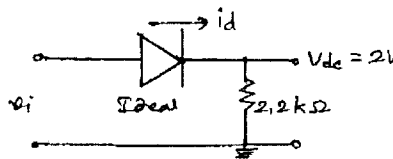


Fig.Q1(a)

- b. Determine v_0 for the network shown in Fig.Q1(b). (06 Marks)

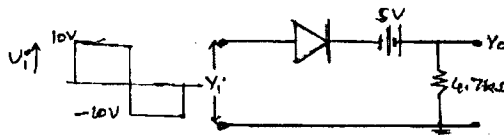


Fig.Q1(b)

- c. Sketch v_0 for the network shown in Fig.Q1(c). (06 Marks)

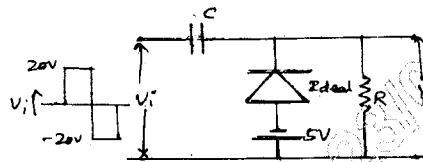


Fig.Q1(c)

- 2 a. Using exact analysis, obtain the Q-point values for the voltage-divider bias circuit. (08 Marks)
 b. Obtain the expression for $S(I_{CO})$ for an emitter-bias circuit and determine its value for the circuit with $R_B = 470 \text{ k}\Omega$, $R_E = 2.2 \text{ k}\Omega$, $R_C = 3.3 \text{ k}\Omega$, $V_{CC} = 12\text{V}$ and $\beta = 100$. (06 Marks)
 c. For the circuit shown in Fig.Q2(c), determine the values for R_1 and R_C . (06 Marks)

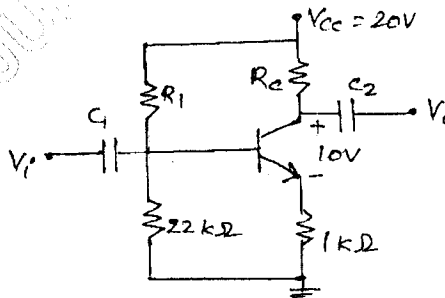


Fig.Q2(c)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any marking of identification applied to evaluator and for computer use written on 47.8 - 50 will be treated as malpractice.

- 3 a. Derive the equations for Z_i , Z_o and A_v for fully bypassed common emitter RC-coupled amplifier. (08 Marks)
- b. Compare Z_i , Z_o and A_v of a RC coupled amplifier with emitter follower and explain why emitter follower is called as impedance matching network. (06 Marks)
- c. For the circuit shown in Fig.Q3(c), find Z_i , Z_o and A_v . (06 Marks)

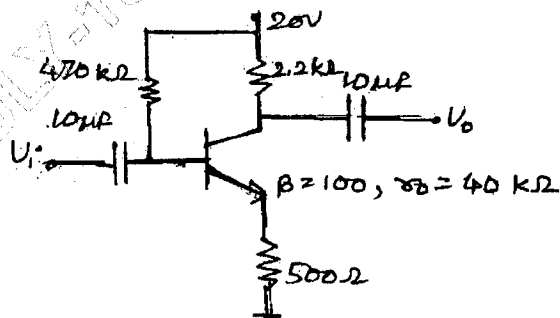


Fig.Q3(c)

- 4 a. Draw the frequency response of RC coupled amplifier and explain high-pass action at low frequencies and low-pass action at high frequencies with relevant equations and Bode plots. (08 Marks)
- b. Draw the high frequency equivalent circuit for RC coupled amplifier and obtain expressions for f_{Hi} and f_{Ho} . (06 Marks)
- c. Determine f_{Cs} and f_{Cc} for circuit with,
 $C_S = 10\mu F$, $C_E = 20\mu F$, $C_C = 1\mu F$, $R_S = 1k\Omega$, $R_1 = 40k\Omega$, $R_2 = 10k\Omega$, $R_E = 2k\Omega$, $R_C = 4k\Omega$, $R_L = 2.2k\Omega$, $\beta = 100$, $r_0 = \infty$, $V_{CC} = 20V$. (06 Marks)

PART - B

- 5 a. Explain the advantages of employing negative feedback in an amplifier. (06 Marks)
- b. Derive an equation for Z_i and A_v for a Darlington emitter follower. (08 Marks)
- c. For cascaded stages shown in Fig.Q5(c), determine :
 i) Loaded gain for each stage
 ii) Total gain for the system A_v and A_{vs} . (06 Marks)

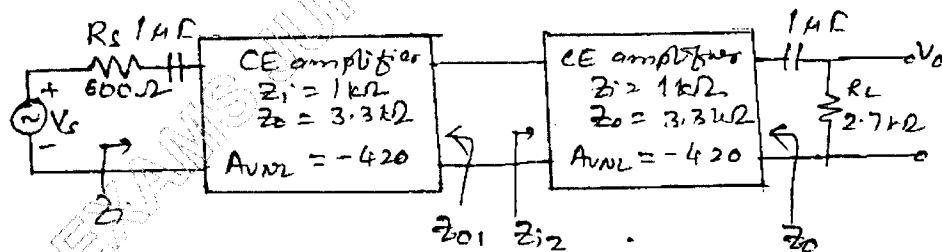


Fig.Q5(c)

- 6 a. Derive the expression for maximum percentage efficiency for a seriesfed class-A power amplifier. (08 Marks)
- b. Calculate the second harmonic distortion for an output waveform with $V_{CEQ} = 10V$, $V_{CE_{min}} = 1V$, $V_{CE_{max}} = 18V$. (06 Marks)
- c. Draw the circuit of a class-B push-pull amplifier and explain the working. Explain why cross-over distortion occurs in class-B and how it is overcome. (06 Marks)
- 7 a. With a neat circuit diagram, explain the principle of operation of RC phase-shift oscillator with necessary equations. (08 Marks)
- b. Explain the working of transistor crystal oscillator in series resonant mode. (06 Marks)
- c. Design a Weinbridge oscillator for a frequency of 4KHz. (06 Marks)
- 8 a. Derive equations for Z_i , Z_o and A_v for JFET fixed bias configuration, with source resistor bypassed. (08 Marks)
- b. For JFET amplifier shown in Fig.Q8(b), find Z_i , Z_o and A_v . (08 Marks)

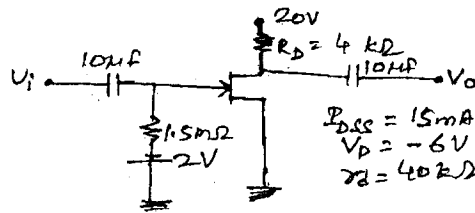


Fig.Q8(b)

- c. Explain the graphical determination of g_m . (04 Marks)
